REMARKS

I. Formal Matters.

Claims 1-7, 9 and 12-23 are currently pending in this application, all of which stand finally rejected. Initially, Applicant thanks the Examiner for withdrawing the prior objection to claim 22.

II. Claim Objection.

The Examiner objects to claim 23 due to a typographical error, which has been remedied via the foregoing amendment. Accordingly, withdrawal of the objection to claim 23 is respectfully requested.

III. 35 U.S.C. §102(e).

The Examiner rejects claim 23 as allegedly being anticipated by *Sung* (U.S. Patent No. 5,858,831) under 35 U.S.C. §102(e).

Sung teaches the formation of a patentably distinguishable semiconductor device formed by a patentably distinguishable method compared to the method of claim 23. *Sung* teaches forming a first polysilicon film (37) on an upper surface of the interlayer film (34/29) and a second polysilicon film (37) on an inner wall of the groove (36) (col. 7, lines 45-54). Subsequently, *Sung* teaches forming a capacitor dielectric layer (38) on the first and second polysilicon layer (37) (col. 7, line 54 -col. 8, line 4). *Sung* teaches forming an HSG layer upon first and

second polysilicon layer (37) as optional (col. 7, lines 50-54). Next, *Sung* teaches a CMP process *to remove* the first polysilicon layer (37) (on the upper surface of inter layer film (34/27)) *and to remove* capacitor dielectric layer (38) from the upper surface of the interlayer film (34/27). This process is clearly stated, "resulting in polysilicon...layer (37), and capacitor dielectric layer (38) residing only in storage node openings (36) (col. 8, lines 4-8; Fig. 18). Finally, *Sung* teaches a polysilicon [upper electrode] layer (39) as being formed across the exposed surface, which comprises an inner groove wall capacitor dielectric layer (38) *and* an upper interlayer surface (34/27). This is clearly shown in Figs. 19 and 20 and taught in col. 7, line 34 to col. 8, line 44).

Claim 23 is distinguishable from the teaching of *Sung* on two grounds. *Sung* discloses forming a capacitor dielectric layer only on the polysilicon film, where said polysilicon film is present both in the walls and on the upper surface of the interlayer. In contrast to *Sung*, claim 23 requires forming a capacitor dielectric layer on [the second HSG] in the inner walls of the groove *and* on the upper exposed surface of the interlayer film. *Sung* fails to disclose forming a capacitor dielectric layer on an upper surface of the interlayer.

Second, claim 23 requires forming the upper electrode on the capacitor dielectric film, said upper electrode being free from contacting said interlayer film. *Sung* discloses forming a polysilicon layer [upper electrode] (39) across the exposed surface, which is the capacitor dielectric layer in the inner walls of the groove and the upper surface of interlayer (34/27). This is clearly shown in Figs 19 and 20 and taught in col. 8, lines 9-44 of *Sung*. Applicant's method

results in both a capacitor dielectric layer and an upper electrode layer upon the upper surface of the interlayer with the upper electrode formed on the capacitor dielectric layer (Fig. 7G; claims 1 and 23). *Sung*'s method results in an upper electrode layer upon the upper surface of the interlayer and upon the capacitor dielectric layer (Figs. 19 and 20)

At least for failing to disclose forming an upper electrode on the capacitor dielectric film, said upper electrode being free from contacting said interlayer film, the rejection of claim 23 as being anticipated by *Sung* under 35 U.S.C. §102(e) should be withdrawn. Further, as presented in the first grounds for distinguishment, *Sung* fails to disclose forming a capacitor dielectric layer on an upper surface of the interlayer, where *Sung* teaches forming a capacitor dielectric layer only upon a polysilicon layer. At least for failing to disclose forming a capacitor dielectric layer on an upper surface of the interlayer, the rejection of claim 23 as being anticipated by *Sung* should be withdrawn.

IV. 35 U.S.C. §103(a).

The Examiner rejects claims 1-7, 9 and 12-22 as allegedly being unpatentable over *Sung* in view of Applicant's Admitted Prior Art (*AAPA*) and JP-A-11-284139 (*JP '139*).

Regarding claims 1 and 16, the Examiner acknowledges that *Sung* does not teach forming a capacitor dielectric film 38 on the second HSG film after removing the first HSG and the first polysilicon film from the CMOS logic portion (FOA page 6). Therein, the Examiner relies on *JP '139* to teach this element.

Applicant respectfully submits that *JP '139* teaches removing a first HSG and a first polysilicon layer film from an upper surface interlayer 44A (page 14, paragraph 2; Fig. 6.). However, *JP '139* further teaches that after this step, the remaining portions of the interlayer (44A) (and plug 54A) are removed (page 14, paragraph 3; Fig. 7). Subsequently, a capacitor dielectric and an upper electrode are formed on the resulting surface, said surface comprising a second inner groove HSG, an exposed first polysilicon outer wall (50), and an exposed etch barrier layer 34 (page 12, paragraph 3; Figs. 3 and 7). The resulting device is distinguishable from that claimed by Applicant and taught by *Sung*. *JP '139* removes the first HSG and first polysilicon layer *and* the remaining interlayer before forming a capacitor dielectric layer on the inner walls and outer walls of the groove, forming *a crown* capacitor. *JP '139* teaches that removing the first HSG prevents HSG grains from falling outside grooves, [given the narrow groove wall and missing interlayer] (*JP '139* page 16, second paragraph). The teachings of *JP '139* are conducive to forming a crown capacitor.

The Examiner asserts that the motivation to combine an interim series of steps taught in *JP '139* into a processing method taught by *Sung* is that so doing would provide better planarization for the subsequent processing steps.

However, *Sung* already teaches a planarization step, CMP, after forming the capacitor dielectric layer on the first and second polysilicon layer (col. 8, lines 4-8). *Sung* teaches a CMP (planarization) step comprising polishing down the first capacitor dielectric layer and the first polysilicon layer *in a single CMP step*. If one were to incorporate the teachings of *JP '139* and

Sung and still obtain *Sung*'s device, one would incur an additional CMP step, one upon the first polysilicon layer and first HSG, and a second CMP step upon the first capacitor dielectric layer. There is no evidence to suggest that a two step CMP process results in better planarization for subsequent steps. There is no evidence to suggest that the interim planarization/CMP process is necessary or desirable. There is no motivation to perform the interim CMP step of *JP '139* in combination with the teachings of *Sung*. If improved planarization for subsequent steps constitutes a legitimate motivation to combine, then one would expect to find increased CMP steps in semiconductor manufacturing at large.

JP '139 had a specific reason to perform CMP upon the first polysilicon layer and the first HSG; this reason is missing from *Sung*. In fact, *Sung* teaches that an HSG layer can be laid down before the capacitor dielectric layer, and *Sung* still fails to teach or suggest the need or desire to remove the HSG layer from the upper surface of the interlayer before laying down the capacitor dielectric layer. Combining *JP '139* and *Sung* is counterintuitive. If anything, *Sung* teaches away from the combination asserted by the Examiner by teaching CMP upon a first polysilicon layer, a first HSG layer, and a first capacitor dielectric in a single step. *AAPA* fails to provide the element lacking in the primary reference. A teaching or suggestion to make the claimed combination of claims 1 and 16 is not present in the prior art. The Examiner fails to make a *prima facie* case of obviousness by failing to provide a viable motivation to combine the prior art. Neither the nature of the problem to be solved, the teachings of the prior art, nor the knowledge of one of ordinary skill in the art provides a motivation to combine the references in

the manner asserted by the Examiner to obtain Applicant's claim (*In re Rouffet*, 149 F.3d 1350, 1357). At least for the lack of motivation to combine *Sung*, *AAPA* and *JP '139*, the rejection of claims 1 and 16 as being unpatentable over *Sung* in view of *AAPA* and *JP '139* should be withdrawn.

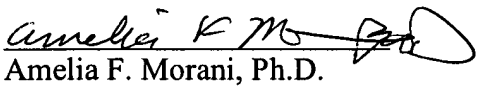
In addition, claims 1 and 16 are patentable on the following grounds. *JP '139* teaches the formation of a first HSG film, a first polysilicon film on an upper surface of an interlayer 44. However, *JP '139* only discloses a general-purpose DRAM device as the prior art of the present invention shown in Fig. 6A. Therefore, a P-MOS and an N-MOS mentioned in the second paragraph at page 9 of *JP '139* only comprise a peripheral circuit (as region 2 in Fig. 6A). Therefore, the Examiner is respectfully requested to withdraw the rejection of claims 1 and 16 under 35 U.S.C. §103(a).

Claims 2-7, 9, 12-15, and 17-22 are asserted as being patentable at least by virtue of their dependence upon an allowable claim.

In view of the preceding amendment and remarks, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby earnestly solicited. If there are any points remaining in issue that the Examiner feels may be best resolved through a personal or telephonic interview, the Examiner is kindly requested to contact the undersigned at the local telephone number listed below.

The USPTO is directed and authorized to charge all required fees (except the Issue/Publication Fees) to our Deposit Account No. 19-4880. Please also credit any over-payments to said Deposit Account.

Respectfully submitted,



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